Thinker Toys™

Preliminary

USER'S MANUAL

SupeRam™ 32K

32K Static Memory

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ADVISEMENT FOR KIT BUILDERS

The kit you have purchased is a complex electronic device and will require a certain level of skill to assemble and thoroughly check out. Persons who do not have a rudimentary knowledge of digital logic or who are not skilled with the use of a soldering iron and a simple volt-ohm-ampmeter should not attempt to assemble this kit.

The warranty provides for replacement of faulty parts for a period of six months from the time of purchase as long as the registration card included with the kit is on file at Thinker Toys. Parts identified as faulty will be replaced without cost by Thinker Toys if they have not been subject to abuse.

Thinker Toys purchases only the highest quality commercially available parts for its products and maintains a thorough quality control program. But no system is perfect and occasionally a part which is faulty or will become faulty will find its way into one of our kits despite our best efforts. In the event one of these faulty parts is in this kit it will be the primary responsibility of the kit builder with the help of the instructions included here to identify this part. Before beginning to construct this kit you should read the assembly instructions thoroughly. Afterwards you should decide whether your level of skill and knowledge are sufficient to carry through the necessary trouble-shooting procedures in the event the kit does not function properly after assembly.

By far and away the biggest single reason a kit will not function after assembly is that it has not been constructed properly. Pins bent under a device while inserting it in a socket accounted for a large portion the faulty kits received for repair during 1978. However, even a simple problem such as this takes as much time to identify and repair as a much more serious problem such as a board short.

INTRODUCTION

The SuperRam 32K is the latest in the line of memories from Thinker Toys. As with the original ECONORAM and the Thinker Toys 8K and 16K memories, this board, too is the design of George Morrow. SuperRam 32K uses the National 5257-3L or the TI equivalent 40L44-25 4Kx1 NMOS memory chips and can be run to 2 MHz or 4MHz (for Z-80 systems). It is fully buffered and each 16K block is independently addressable and write protectable. Like all Thinker Toy products, SuperRam 32K meets the Proposed IEEE S-100 Standard and will work with any computer meeting these specifications.

We at George Morrow's Thinker Toys hope you will enjoy your new SuperRam 32K memory unit.

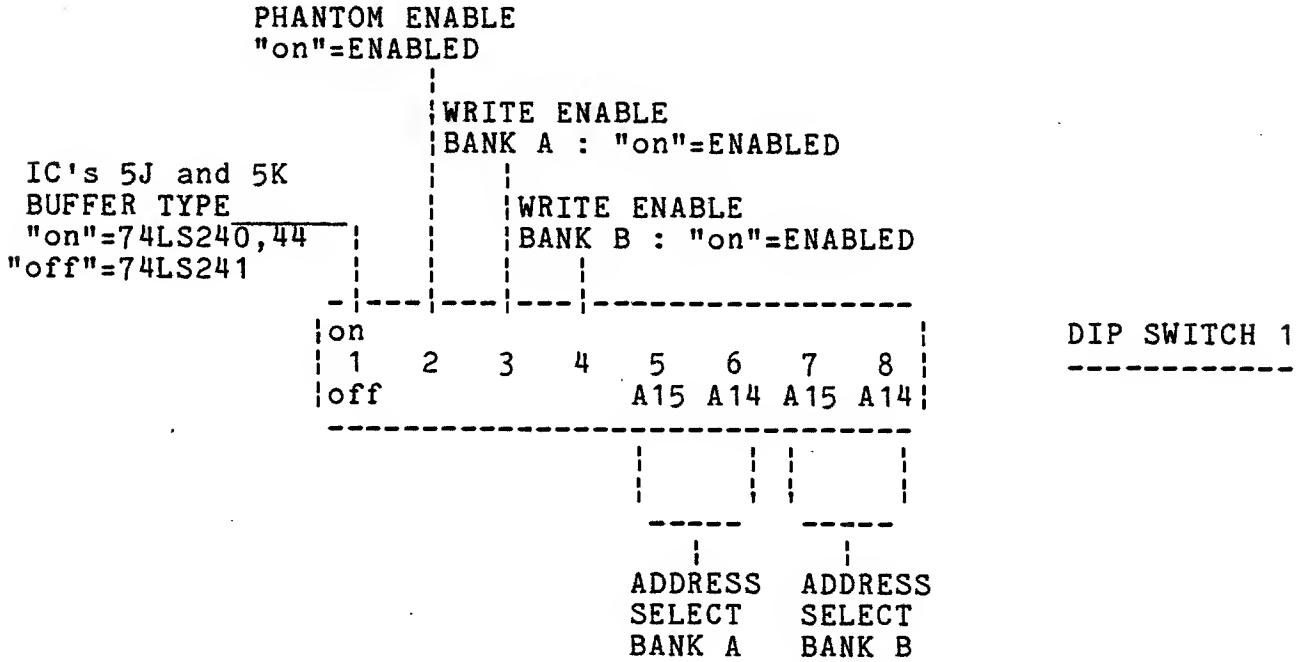
OPERATING INSTRUCTIONS

Important note: To aviod electrical damage to your SuperRam memory board, turn OFF the power in your computer before installing or removing the memory board.

ADDRESSING

The 32K SuperRam is configured as two blocks of 16K bytes each. Each of the 16K blocks can be addressed on a 16K boundary. Since the S-100 bus currently supports a 64K byte address space, there are four possible locations for either of the two 16K blocks. They are: 0000 to 3FFFH, 4000 to 7FFFH, 8000 to BFFFH, and C000 to FFFFH.

The function of each of the switches and the DIP Switch array at the top of the board is shown below.



For addressing purposes, an address selection switch that is in the ON position means that the address bit matched is a 0. That is, if both switches are ON, the block of memory responds to any address in the range 0000 to 3FFFH (000:000 to 077:377Q).

ADDRESSING TABLE

LEFT SWITCH	RIGHT SWITCH	HEX ADDRESS	OCTAL ADDRESS
ON	ON	0000	000:000
ON	OFF	4000	100:000
OFF	ON	8000	200:000
OFF	OFF	C000	300:000

WRITE PROTECTION

Switches 3 and 4 are used to write enable or disable the two banks of memory. If the switch is ON, the bank is write enabled. If it is off, the bank is write protected.

PHANTOM OPTION

Switch 2 is used to enable or disable the PHANTOM line disable option. If the switch is ON, the board will respond to the PHANTOM signal and turn itself off when this signal is in its low active state. If the switch is OFF, the board will not be affected by the state of the PHANTOM line.

A word of warning! At least one of the CPU cards using the Z-80 microprosessor chip have used the line 68 (PHANTOM) as a dynamic memory refresh signal. If your CPU board does this, leave the phantom switch in the OFF position; otherwise the board will be disabled during the first byte of an op-code fetch cycle - a state of affairs guarenteed to cause trouble.

DATA BUFFER SELECTION

Switch 1 is used to allow the board to utilize one of several different kinds of data buffer/driver chips. The pair of data buffers included with this unit may be any of the following devices: 74LS240, 74LS244, or 74LS241. If there are 74LS240s or 74LS244s at positions 5J and 5K switch 1 must be in the ON position. If on the other hand, 74LS241s are in these positions, switch 1 must be in the OFF position.

ADDRESSING TABLE

LEFT SWITCH	RIGHT SWITCH	HEX ADDRESS	OCTAL ADDRESS
ON	ON	0000	000:000
ON	OFF	4000	100:000
OFF	ON	8000	200:000
OFF	OFF	C000	300:000

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MEMORY DIAGNOSTIC

The memory test described below was designed by Phil Meads of William Brobeck Associates to exercise the most sensitive circuitry of the memory chips -- the address buffers. The test starts from the middle and works its way outward alternately to the top and bottom of memory. This type of test inverts the address lines more often than sequential ones. This continual inversion process punishes and eventually breaks down weak or faulty address buffers in the device.

USUNG THE TEST

The test itself must be placed in an area which is different than the location of the board(s) to be tested. The test starts on a page boundary to make the task of relocating the binary code easier.

There are two parameters in the test to be set by the user:

(1) The number of 4K blocks to be tested -- keep in mind that there are eight 4K blocks per board. This constant is called BLKCNT and is located at the eleventh byte of the test.

(2) The starting page number of the lowest 4K block to be tested is called PAGENO and is located at the ninth byte of the test.

When testing more than one 4K block of memory, be sure that they occupy contiguous memory.

The page number of the position of the test itself must be entered wherever a YYY (octal) or a YY (hex) occurs in the test listing. This is necessary because JMP and CALL instructions need both the page number and the location within the page to execute correctly.

The only other thing to remember when loading the test is that it must be placed at the starting address of a page.

Start the test at the first instruction. Once started, the test will run continuously unless an error is detected. If the test encounters an error, all the data pertinent to this error is stored in the last ten locations of the test (see the listing that follows). After storing this error information, the test comes to a dynamic halt at the label STALL. The test may be restarted by stopping the computer and restarting it at the POP PSW instruction following JMP STALL. The user may also restart the test from the beginning.

If errors indicate the board is malfunctioning, carefully analyze the error information at the end of the test to determine which memory chips are faulty so that they can be replaced. Keep in mind that if the unit has been purchased assembled and tested and is still in warranty it may be returned to Thinker Toys for repair without charge.

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Octal)

```
YYY  000 061 175 YYY    START  LXI   SP,STACK   INITIALIZE STACK POINTER
     003 001 000 000           LXI   B,0        INITIALIZE CYCLE COUNT
     006 305           NEWCYL  PUSH  B          UPDATE CYCLE COUNT
     007 006 100               MVI   B,PAGENO   STARTING ADDR OF TEST MEM
     011 016 002               MVI   C,BLKCNT   # OF 4K BLOCKS TO TEST
     013 041 377 007   LOOP    LXI   H,7:377Q   HALF SIZE OF MEMORY -1
     016 170                   MOV   A,B
     017 204                   ADD   H          CALCULATE MIDDLE
     020 147                   MOV   H,A          OF CURRENT BLOCK
     021 345                   PUSH  H          SAVE INITIAL ADDRESS
     022 315 114 YYY   WRITE   CALL  TWORD      GET TEST WORD
     025 167                   MOV   M,A        STORE
     026 315 123 YYY           CALL  COMP       COMPLEMENT ADDRESS
     031 315 114 YYY           CALL  TWORD      GET TEST WORD
     034 167                   MOV   M,A        STORE
     035 315 134 YYY           CALL  INCR       COMPLEMENT & DECREMENT
     040 302 022 YYY           JNZ   WRITE        ADDRESS
     043 341                   POP   H          RECOVER INITIAL ADDRESS

YYY  044 315 114 YYY   READ    CALL  TWORD      GET TEST WORD
     047 256                   XRA   M          COMPARE
     050 304 145 YYY           CNZ   ERROR
     053 315 123 YYY           CALL  COMP       COMPLEMENT ADDRESS
     056 315 114 YYY           CALL  TWORD      GET TEST WORD
     061 256                   XRA   M          COMPARE
     062 304 145 YYY           CNZ   ERROR
     065 315 134 YYY           CALL  INCR       COMPLEMENT & DECREMENT
     070 302 044 YYY           JNZ   READ         ADDRESS

YYY  073 076 020               MVI   A,20Q      ADVANCE
     075 200                   ADD   B            THE
     076 107                   MOV   B,A          BLOCK
     077 015                   DCR   C          DECREMENT BLOCK COUNT
     100 302 013 YYY           JNZ   LOOP
     103 173                   MOV   A,E        CALCULATE NEW
     104 306 207               ADI   135          BASE FOR
     106 137                   MOV   E,A          TEST WORD
     107 301                   POP   B
     110 003                   INX   B          INCREMENT CYCLE COUNT
     111 303 006 YYY           JMP   NEWCYL

     114 175           TWORD   MOV   A,L        GET LOWER BYTE OF ADDRESS
     115 007                   RLC              ROTATE
     116 207                   ADD   A          SHIFT
     117 204                   ADD   H          ADD HIGHER BYTE OF ADDR
     120 203                   ADD   E          ADD BASE
     121 127                   MOV   D,A        SAVE TEST WORD
     122 311                   RET
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Octal)

```
YYY  000 061 175 YYY     START  LXI   SP,STACK   INITIALIZE STACK POINTER
     003 001 000 000            LXI   B,0        INITIALIZE CYCLE COUNT
     006 305            NEWCYL  PUSH  B          UPDATE CYCLE COUNT
     007 006 100                MVI   B,PAGENO   STARTING ADDR OF TEST MEM
     011 016 002                MVI   C,BLKCNT   # OF 4K BLOCKS TO TEST
     013 041 377 007    LOOP    LXI   H,7:377Q   HALF SIZE OF MEMORY -1
     016 170                    MOV   A,B
     017 204                    ADD   H          CALCULATE MIDDLE
     020 147                    MOV   H,A          OF CURRENT BLOCK
     021 345                    PUSH  H          SAVE INITIAL ADDRESS
     022 315 114 YYY    WRITE   CALL  TWORD      GET TEST WORD
     025 167                    MOV   M,A        STORE
     026 315 123 YYY            CALL  COMP       COMPLEMENT ADDRESS
     031 315 114 YYY            CALL  TWORD      GET TEST WORD
     034 167                    MOV   M,A        STORE
     035 315 134 YYY            CALL  INCR       COMPLEMENT & DECREMENT
     040 302 022 YYY            JNZ   WRITE        ADDRESS
     043 341                    POP   H          RECOVER INITIAL ADDRESS

YYY  044 315 114 YYY     READ    CALL  TWORD      GET TEST WORD
     047 256                    XRA   M          COMPARE
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     061 256                    XRA   M          COMPARE
     062 304 145 YYY            CNZ   ERROR
     065 315 134 YYY            CALL  INCR       COMPLEMENT & DECREMENT
     070 302 044 YYY            JNZ   READ        ADDRESS

YYY  073 076 020                MVI   A,20Q     ADVANCE
     075 200                    ADD   B            THE
     076 107                    MOV   B,A          BLOCK
     077 015                    DCR   C          DECREMENT BLOCK COUNT
     100 302 013 YYY            JNZ   LOOP
     103 173                    MOV   A,E        CALCULATE NEW
     104 306 207                ADI   135          BASE FOR
     106 137                    MOV   E,A          TEST WORD
     107 301                    POP   B
     110 003                    INX   B          INCREMENT CYCLE COUNT
     111 303 006 YYY            JMP   NEWCYL

     114 175            TWORD   MOV   A,L        GET LOWER BYTE OF ADDRESS
     115 007                    RLC              ROTATE
     116 207                    ADD   A          SHIFT
     117 204                    ADD   H          ADD HIGHER BYTE OF ADDR
     120 203                    ADD   E          ADD BASE
     121 127                    MOV   D,A        SAVE TEST WORD
     122 311                    RET
```

```
YYY  123  174           COMP   MOV   A,H      COMPLEMENT THE UPPER
     124  356 017               XRI   17Q        BYTE ADDRESS
     126  147                   MOV   H,A        WITH RESPECT TO MEM SIZE
     127  175                   MOV   A,L      COMPLEMENT THE LOWER
     130  356 377               XRI   377Q       BYTE OF THE
     132  157                   MOV   L,A        ADDRESS
     133  311                   RET

YYY  134  315 123 YYY  INCR   CALL  COMP     RESTORE ADDR TO NORMAL SIZE
     137  053                   DCX   H        DECREMENT
     140  300                   RNZ            TEST IF LOWER BYTE ZERO
     141  170                   MOV   A,B      TEST UPPER BYTE EQUAL
     142  075                   DCR   A          TO BLOCK
     143  274                   CMP   H          BOUNDARY
     144  311                   RET

YYY  145  345           ERROR  PUSH  H        SAVE ERROR ADDRESS
     146  305                   PUSH  B        SAVE CURRENT BLOCK
     147  325                   PUSH  D        SAVE TEST WORD
     150  365                   PUSH  PSW      SAVE ERROR BITS
     151  303 151 YYY  STALL  JMP   STALL    DYNAMIC HALT
     154  361                   POP   PSW      RESTORE
     155  321                   POP   D          THE
     156  301                   POP   B          STATE OF
     157  341                   POP   H          THE CPU
     160  311                   RET

YYY  161  000           TABLE  DB    0        FLAGS
     162  000                   DB    0        ACC - ONES ARE ERROR BITS
     163  000                   DB    0        E - CURRENT RANDOM OFFSET
     164  000                   DB    0        D - CURRENT TEST WORD
     165  000                   DB    0        C - CURRENT BLOCK COUNT
     166  000                   DB    0        B - CURRENT BLOCK PAGE
     167  000 000               DW    0        HL - ERROR ADDRESS
     171  000 000               DW    0        RETURN ADDRESS
     173  000 000               DW    0        CYCLE COUNT
     175  000 000         STACK DW    0
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Hex)

```
YY  00   31 7D YY      START  LXI   SP,STACK
    03   01 00 00             LXI   B,0
    06   C5           NEWCYL PUSH  B
    07   06 40                MVI   B,PAGENO
    09   0E 02                MVI   C,BLKCNT
    0B   21 FF 07      LOOP   LXI   H,7:377Q
    0E   78                   MOV   A,B
    0F   84                   ADD   H
    10   67                   MOV   H,A
    11   E5                   PUSH  H
    12   CD 4C YY      WRITE  CALL  TWORD
    15   77                   MOV   M,A
    16   CD 53 YY             CALL  COMP
    19   CD 4C YY             CALL  TWORD
    1C   77                   MOV   M,A
    1D   CD 5C YY             CALL  INCR
    20   C2 12 YY             JNZ   WRITE
    23   E1                   POP   H

YY  24   CD 4C YY      READ   CALL  TWORD
    27   AE                   XRA   M
    28   C4 65 YY             CNZ   ERROR
    2B   CD 53 YY             CALL  COMP
    2E   CD 4C YY             CALL  TWORD
    31   AE                   XRA   M
    32   C4 65 YY             CNZ   ERROR
    35   CD 5C YY             CALL  INCR
    38   C2 24 YY             JNZ   READ

YY  3B   3E 10                MVI   A,20Q
    3D   80                   ADD   B
    3E   47                   MOV   B,A
    3F   0D                   DCR   C
    40   C2 0B YY             JNZ   LOOP
    43   7B                   MOV   A,E
    44   C6 87                ADI   135
    46   5F                   MOV   E,A
    47   C1                   POP   B
    48   03                   INX   B
    49   C3 06 YY             JMP   NEWCYL

YY  4C   7D           TWORD  MOV   A,L
    4D   07                   RLC
    4E   87                   ADD   A
    4F   84                   ADD   H
    50   83                   ADD   E
    51   57                   MOV   D,A
    52   C9                   RET
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Hex)

```
YY  00   31 7D YY      START  LXI   SP,STACK
    03   01 00 00             LXI   B,0
    06   C5           NEWCYL  PUSH  B
    07   06 40                MVI   B,PAGENO
    09   0E 02                MVI   C,BLKCNT
    0B   21 FF 07      LOOP    LXI   H,7:377Q
    0E   78                    MOV   A,B
    0F   84                    ADD   H
    10   67                    MOV   H,A
    11   E5                    PUSH  H
    12   CD 4C YY      WRITE   CALL  TWORD
    15   77                    MOV   M,A
    16   CD 53 YY              CALL  COMP
    19   CD 4C YY              CALL  TWORD
    1C   77                    MOV   M,A
    1D   CD 5C YY              CALL  INCR
    20   C2 12 YY              JNZ   WRITE
    23   E1                    POP   H

YY  24   CD 4C YY      READ    CALL  TWORD
    27   AE                    XRA   M
    28   C4 65 YY              CNZ   ERROR
    2B   CD 53 YY              CALL  COMP
    2E   CD 4C YY              CALL  TWORD
    31   AE                    XRA   M
    32   C4 65 YY              CNZ   ERROR
    35   CD 5C YY              CALL  INCR
    38   C2 24 YY              JNZ   READ

YY  3B   3E 10                MVI   A,20Q
    3D   80                   ADD   B
    3E   47                   MOV   B,A
    3F   0D                   DCR   C
    40   C2 0B YY             JNZ   LOOP
    43   7B                   MOV   A,E
    44   C6 87                ADI   135
    46   5F                   MOV   E,A
    47   C1                   POP   B
    48   03                   INX   B
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    51   57                  MOV   D,A
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```
YY  53   7C          COMP   MOV    A,H
    54   EE 0F              XRI    17Q
    56   67                 MOV    H,A
    57   7D                 MOV    A,L
    58   EE FF              XRI    377Q
    5A   6F                 MOV    L,A
    5B   C9                 RET

YY  5C   CD 53 YY    INCR   CALL   COMP
    5F   2B                 DCX    H
    60   C0                 RNZ
    61   78                 MOV    A,B
    62   3D                 DCR    A
    63   BC                 CMP    H
    64   C9                 RET

YY  65   E5          ERROR  PUSH   H
    66   C5                 PUSH   B
    67   D5                 PUSH   D
    68   F5                 PUSH   PSW
    69   C3 69 YY    STALL  JMP    STALL
    6C   F1                 POP    PSW
    6D   D1                 POP    D
    6E   C1                 POP    B
    6F   E1                 POP    H
    70   C9                 RET

YY  71   00          TABLE  DB     0        FLAGS
    72   00                 DB     0        ACC - ONES ARE ERROR BITS
    73   00                 DB     0        E - CURRENT RANDOM OFFSET
    74   00                 DB     0        D - CURRENT TEST WORD
    75   00                 DB     0        C - BLOCKS LEFT TO TEST
    76   00                 DB     0        B - CURRENT BLOCK PAGE
    77   00 00              DW     0        HL - ERROR ADDRESS
    79   00 00              DW     0        RETURN ADDRESS
    7B   00 00              DW     0        CYCLE COUNT
    7D   00 00          STACK  DW     0
```

PARTS LIST

__	1	5" x 10" printed circuit board
__	1	8" x 10" glossy photograph
__	1	3.3k Ohm 1/4 watt resistor
__	1	SIP resistor array
__	18	By-pass capacitors*
__	5	39 mircofarad tantulum capacitors
__	3	14-pin low profile sockets
__	1	16-pin low profile socket
__	64	18-pin low profile sockets
__	4	20-pin low profile sockets
__	1	8 position DIP switch array
__	4	6-32 x 3/8 machine screws
__	4	6-32 x 1/4 machine nuts
__	4	Heat sinks
__	4	7805/340.5 Monolthic voltage regulators
__	1	74LS10 Triple 3-input NAND gate (5E)
__	1	74LS32 Quad 2-input OR gate (5C)
__	1	74LS138 1 of 8 decoder with enable (5F)
__	2	74LS240/241/244 Tri-state** octal buffer/driver (5J,5K)
__	1	74LS266 Quad 2-input open collector exclusive NOR gate (5B)
__	1	81LS95/96/97/98 Tri-state octal buffer (4M)
__	1	81LS96/98 Tri-state inverting octal buffer (5D)
__	64	MM5257-3L/40L44-25 4K x 1 NMOS static ram

* By-pass capicators may vary from .01 to .1 microfarads depending on current supplies

** Tri-state is a registered trade mark of National Semiconductor

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__	64	18-pin low profile sockets
__	4	20-pin low profile sockets
__	1	8 position DIP switch array
__	4	6-32 x 3/8 machine screws
__	4	6-32 x 1/4 machine nuts
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__	4	7805/340.5 Monolthic voltage regulators
__	1	74LS10 Triple 3-input NAND gate (5E)
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__	1	74LS138 1 of 8 decoder with enable (5F)
__	2	74LS240/241/244 Tri-state** octal buffer/driver (5J,5K)
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__	1	81LS95/96/97/98 Tri-state octal buffer (4M)
__	1	81LS96/98 Tri-state inverting octal buffer (5D)
__	64	MM5257-3L/40L44-25 4K x 1 NMOS static ram

* By-pass capicators may vary from .01 to .1 microfarads depending on current supplies

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ASSEMBLY INSTRUCTIONS

DO NOT INSTALL OR SOLDER ANY PARTS UNTIL YOU HAVE READ THESE INSTRUCTIONS AND UNDERSTAND THEM.

CAUTION - DO NOT SOLDER OR CLIP COMPONENT LEADS WITHOUT USING SAFETY GLASSES!

INSPECTION

Use the parts list included with this manual to make sure that there are no missing items in your kit. Please notify us of any shortages. Be sure to check for missing parts before you start assembly.

CIRCUIT BOARD INSPECTION

Before any parts are installed, the circuit board must be checked for possible short circuits. An Ohm-meter or some other continuity checking device is necessary for this operation. Before checking for short circuits the board should be carefully inspected for obvious physical imperfections such as deep scratches, open traces, or broken traces.

At position 1C (upper left hand side of the board) check for possible shorts between the following pairs of pins:

pin 18 and pin 1
pin 1 and pin 17
pin 17 and pin 2
pin 2 and pin 16
pin 16 and pin 3
pin 3 and pin 15
pin 15 and pin 4
pin 4 and pin 14
pin 14 and pin 5
pin 5 and pin 13
pin 13 and pin 6
pin 6 and pin 12
*pin 12 and pin 7
*pin 7 and pin 11
*pin 11 and pin 8
*pin 8 and pin 9

Repeat this operation at board positions 2C, 3C, 4C, 6C, 7C, 8C, and 9C for the pairs of pins marked with an asterisk.

Next, the power-ground grid should be checked for shorts. Check for shorts between pins 9 & 18 at the following board positions: 1C, 3C, 5C, and 7C. Check that there is no connection between pin #1 and pin #50 of the edge connector.

If shorts have occured at any of the above check points, the circuit board should be returned to Thinker Toys for warranty replacement.

POWER CONTINUITY CHECKS

Check for continuity between the following sets of pins:

(1) 1C pin 18, 2C pin 18, 1L pin 18, and 2L pin 18

(2) 3C pin 18, 4C pin 18, 3L pin 18, 4M pin 20, and 5K pin 20

(3) 5E pin 16, 6C pin 18, 7C pin 18, 6L pin 18, and 7L pin 18

(4) 8C pin 18, 9C pin 18, 8L pin 18, and 9L pin 18

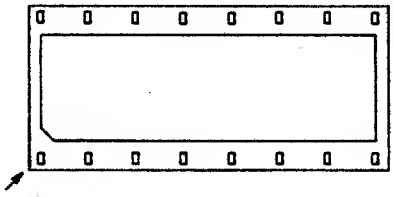
Inspect the power trace on the back side of the board from pin 51 of the edge connector to the inputs of the four 7805 voltage regulators. Inspect the ground traces on the front of the board from pin 50 of the edge connector to the large ground plane/heat sink area at the top of the board.

SOCKETS

A socket has been installed for every integrated circuit on this board. This will facilitate assembly as well as troubleshooting if any is necessary.

PARTS ORIENTATION

In all refecences throughout the instructions, the convention used is that the gold edge connector is the bottom of the board. Orientation identification is molded into the plastic of the sockets either with numbers or in a manner illustrated below.



This orientation mark or an embossed "1" identifies where pin #1 of the integrated circuit is to be positioned when inserted in the socket. The sockets should be inserted in the board so that the orientation mark is in the lower left hand corner.

If shorts have occured at any of the above check points, the circuit board should be returned to Thinker Toys for warranty replacement.

POWER CONTINUITY CHECKS

Check for continuity between the following sets of pins:

(1) 1C pin 18, 2C pin 18, 1L pin 18, and 2L pin 18

(2) 3C pin 18, 4C pin 18, 3L pin 18, 4M pin 20, and 5K pin 20

(3) 5E pin 16, 6C pin 18, 7C pin 18, 6L pin 18, and 7L pin 18

(4) 8C pin 18, 9C pin 18, 8L pin 18, and 9L pin 18

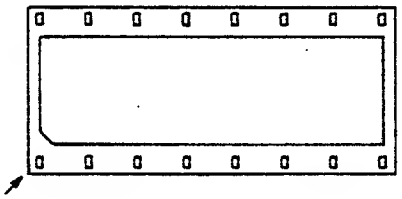
Inspect the power trace on the back side of the board from pin 51 of the edge connector to the inputs of the four 7805 voltage regulators. Inspect the ground traces on the front of the board from pin 50 of the edge connector to the large ground plane/heat sink area at the top of the board.

SOCKETS

A socket has been installed for every integrated circuit on this board. This will facilitate assembly as well as troubleshooting if any is necessary.

PARTS ORIENTATION

In all refecences throughout the instructions, the convention used is that the gold edge connector is the bottom of the board. Orientation identification is molded into the plastic of the sockets either with numbers or in a manner illustrated below.



This orientation mark or an embossed "1" identifies where pin #1 of the integrated circuit is to be positioned when inserted in the socket. The sockets should be inserted in the board so that the orientation mark is in the lower left hand corner.

The tantulum capacitor in position 1B is to be inserted with the red band to the right. The remaining four tantulum capicators in positions 2B, 4B, 7B, and 9B are to be placed with the red band to the left.

The DIP switch at the top of the board is to be positioned with switch #1 to the left.

The SIP (single-in-line pack) resistor array has a dot at one end. The pin associated with this dot is the common point of the nine resistors in this package and must be to the left when the part is soldered to the board.

SOLDERING AND SOLDER IRONS

The most desirable soldering iron for a complex electronic kit such as the SuperRam 32K is a constant temperature device with an element regulated at 650 degrees F. The tip should be fine so that it Can be brought in intimate contact with the small pads of the circuit board. Both Unger and Weller have excellent products which fit the above requirements.

There are three important soldering requirements for building this kit:

1. Do not use an iron that is too cold (less than 600 degrees F) or too hot (more than 750 degrees F).

2. Do not apply the iron to a pad for extended periods.

3. Do not apply excessive amounts of solder.

The proper procedure for soldering components to the circuit board is as follows:

1. Bring the iron in contact with both the component lead and the pad.

2. Apply a small amount of solder at the point where the iron, component lead, and pad all make contact.

3. After the initial application of solder has been accomplished with the solder flowing to the pad and component lead, the heat of the iron will have transferred to both the pad and the lead. Apply a small amount of additional solder to cover the joint between the pad and the lead. DO NOT PILE SOLDER ON THE JOINT! EXCESSIVE HEAT AND SOLDER IS ONE OF THE MOST COMMON CAUSES OF BOARD SHORTS AND SOLDER BRIDGES.

IF FOR ANY REASON IT BECOMES NECESSARY TO REMOVE A COMPONENT WHICH HAS BEEN SOLDERED TO THE BOARD, FIRST CLIP THE LEADS OF THAT COMPONENT. THEN APPLY HEAT FOR SOLDER SUCKER OR WICK TO THE SIDE OF THE PAD WITH A LEAD COMING TO IT. THIS WILL REDUCE THE CHANCES OF LIFTING A PAD.

PARTS INSTALLATION

Install parts in the following sequence:

3.3k Ohm resistor (R1).

14-pin sockets (3) in positions 5B, 5C, and 5E; pin #1 to the lower left.

16-pin socket (1) in position 5F; pin#1 to the lower left.

20-pin sockets (4) in positions 5D, 5J, 5K, and 5M; pin#1 to the lower left.

18-pin sockets (64) in positions 1C - 1L, 2C - 2L, 3C - 3L, 4C - 4L, 6C - 6L, 7C - 7L, 8C - 8L, and 9C - 9L; pin #1 to the lower left.

39 microfarad tantulum capicator C23 with the orientation mark (red band) to the right. Bend the axial leads to a width of .6".

39 microfarad tantulum capicators C1, C2, C3, and C4 with the orientation mark (red band) to the left. Bend the axial leads to a width of .6".

SIP resistor array between positions 5A and 5B. Be sure that the orientation dot at one end of the device is to the left before the part is soldered to the board.

By-pass capicators C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, and C22.

DIP switch in position 5A with switch #1 to the left.

7805/340.5 5-volt regulators (4) by bending the leads, inserting and hand tightening the nut and screw through the circuit board, heat sink and the regulator in that order. Solder the leads. If heat sink grease is available, apply a thin film between the board, heat sink, and regulator before applying the screw and nut. Finally, tighten the nut and screw.

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3.3k Ohm resistor (R1).

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THEORY OF OPERATION

ADDRESS SELECT LOGIC

The SupeRam 32K is configured as two 16K blocks of memory. The board has circuitry which allows both of these blocks to be independently addressed. Each block uses half of a 74LS266 open collector quad exclusive-Nor pack and two switches of an eight position DIP switch array to select one of 4 possible 16K boundaries at which the block is to be located.

One input of each of the two gates is connected to address lines A15 and A14 respectively. The other input is connected to an address select switch and a pull-up resistor. If the switch is open, the pull-up resistor forces a logic "1" to one input of the exclusive-Nor gate.

The outpput transistor of this gate will be in the OFF state if and only if the corresponding address line connected to the other input is also at a logic "1" state.

If the switch is closed, the input to the gate is grounded (logic "0"). In this case the output transistor of the gate will be in the OFF state if and only iff the corresponding address line connected to the other input is also at a logic "0" state.

The two outputs of these exclusive-Nor gates are connected together along with a pull-up resistor to 5 volts.

If both the output transistors of the 74LS266 gates are in the OFF state the common output node will be at a logic "1". This common output node will be at a logic "1" when the logic levels on address lines A15 and A14 independently match the logic levels determined by the switch associated with each line. If there are any mismatches, one or both of the output transistors of the exclusive-Nor gates will be turned ON (i.e. conducting to ground) and the common node will be at a logic "0".

There are two of these common output nodes. They form the input to a 74LS32 OR gate whose output is labeled SEL. When the SEL signal is high, one of the 2 16K blocks of memory will be selected if the status signals SWO, SOUT, SMEM, and (conditionally) $\overline{\text{PHANTOM}}$ are at the appropriate levels to indicate a memory reference bus cycle.

BOARD SELECTION LOGIC

In order to reference one of the two 16K blocks on the board there must be a match in the address lines and the address selection switches. But this is not enough. The only bus cycles which the board will respond to are memory references.

$\overline{SWO}$ is a status signal which is active (logic "0") during bus cycles which transfer data from the CPU to a bus slave (memory, I/O, etc.). SOUT is active (logic "1") when the CPU is transferring data to an I/O device. Thus the CPU is writing into memory when SOUT and $\overline{SWO}$ are both in a logic "0" state. When the CPU is reading memory, SMEMR is active (logic "1")

The signal MEM OP- memory operation- is a logic 1 whenever the CPU is performing a memory read or a memory write bus cycle and is derived from the SMEMR, SOUT, and $\overline{SWO}$ signals.

$\overline{PHANTOM}$ is active (logic "0") when phantom ROM or other exceptional memory must usurp the bus and lock out normal memory to furnish the CPU with special instructions. This is most common during power-up when the CPU's program counter is forced to zero.

Whenever $\overline{PHANTOM}$ is a logic 1 (inactive), MEM OP is a logic 1 (active), and SEL is a logic "1" (active), the board will be selected. Banks 0,1,2 or 3 will be selected whenever SEL B is a logic "0" (inactive). Otherwise banks 4,5,6 or 7 will be selected.

DATA TRANSFER LOGIC

PDBIN is the data input strobe signal. The CPU drives this line high during the period of a bus cycle when an addressed peripheral is to place its data on the input lines of the SupeRam 32K board. The PDBIN signal turns on the tri-state** drivers to the CPU's input data lines whenever the board is selected. This logic is implemented through a three input Nand gate at position 5E.

Both $\overline{PWR}$ and MWRITE are strobe signals active when the CPU transfers data to a peripheral device. $\overline{PWR}$ is the logic "0" strobe for memory writes only. However not all CPU's generate the MWRITE signal. On both the original ALTAIR and IMSAI machines, the MWRITE signal is generated by the front panel.

The only time information can be written into the MM5257-3L/40L44-25 memory chips is when BOTH the chip select ($\overline{CS}$) and the write enable ($\overline{WE}$) inputs are at a logic "0" level. The $\overline{CS}$ inputs are connected to $\overline{BANK0}$, $\overline{BANK1}$, $\overline{BANK2}$, $\overline{BANK3}$, $\overline{BANK4}$, $\overline{BANK5}$, $\overline{BANK6}$, or $\overline{BANK7}$ signals and are low only when the proper block of memory on the board is selected. The $\overline{WE}$ inputs are connected to the $\overline{WRITEA}$ or $\overline{WRITEB}$ signals. These signals are low whenever either of the data output strobes is active AND the write enable switch corresponding to the proper block of memory is closed. Thus, memory must be write enabled AND selected before it can be written.

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Morrow Designs, Inc.

Thinker Toys™ 5221 Central Avenue, Richmond, CA 94804 (415) 524-2101

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KITS - Parts, including the printed circuit boards, purchased in kit form are warranted for a period of ninety (90) days from the invoice/purchase date. If a board, which was purchased in kit form, is returned for testing or repair, a minimum service charge of $35. will be assessed.

ASSEMBLED BOARDS - Parts, including the printed circuit boards, purchased as factory assebmlies, are warranted for a period of six (6) months from the invoice/purchase date. Out-of-Warranty boards returned for testing of repair will be assessed a minimum of $35. service charge. If the charge to repair will exceed $35., the customer will be notified prior to the actual repair.

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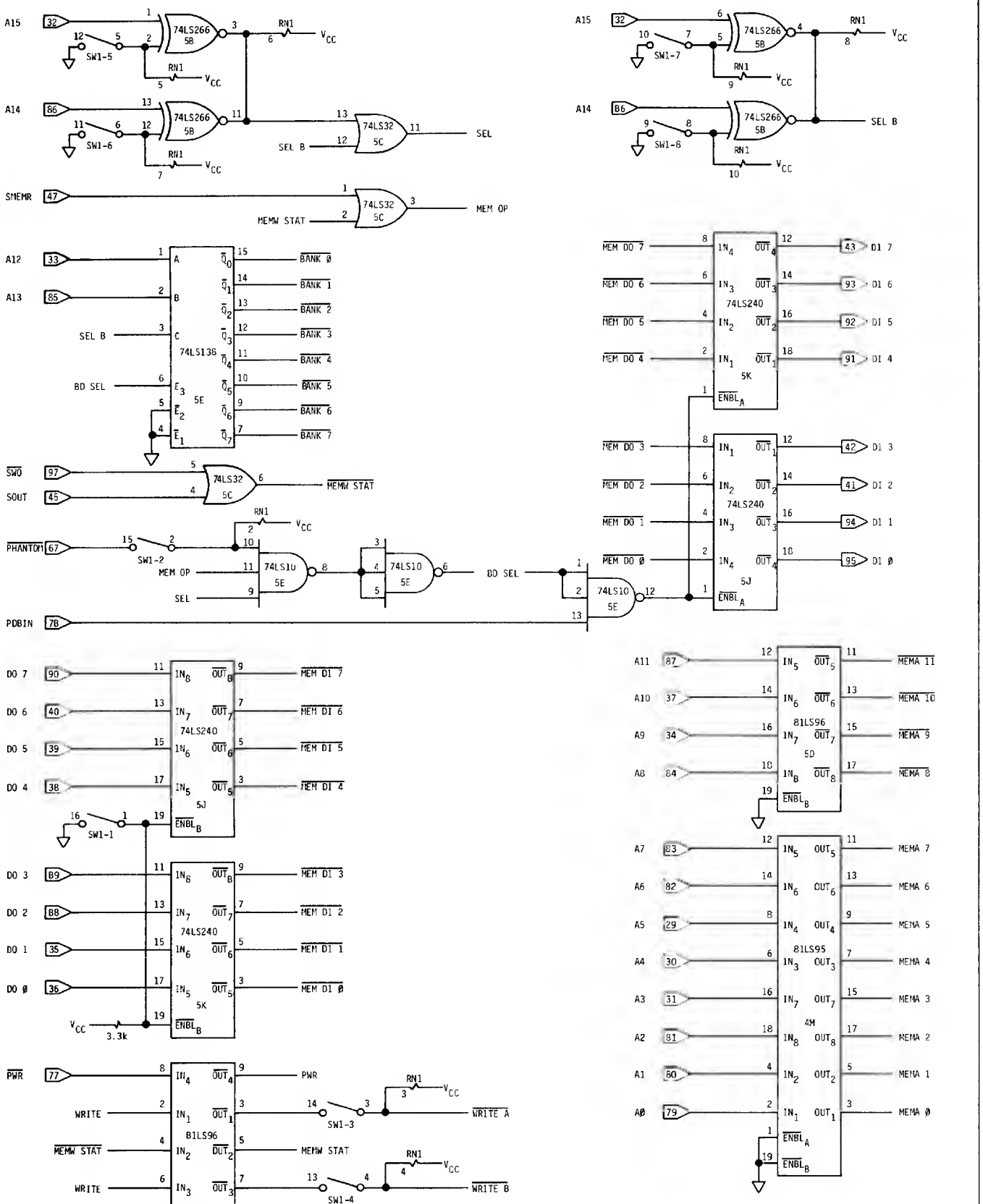
RETURN PROCEDURE - A COPY OF THE INVOICE OR PROOF OF ORIGINAL PURCHASE IS REQUIRED AND MUST ACCOMPANY THE ITEM FOR IN-WARRANTY SERVICE. Items returned without proof of original purchase will be sent back, shipping charges collect. A description of the problem must accompany the returned item. Shipment must be made prepaid to Morrow Designs Inc. Repaired items will be shipped via U.P.S. surface. Shipment by air requires payment of the additional charges. Morrow Designs Inc. is not responsible for any consequential damages of for damage incurred in transit.

The foregoing warranty is in lieu of all other warranties either expressed or implied and, in any event, is limited to product repair or replacement.

Effective February 1, 1980

Specifications, terms, and pricing are subject to change without notice.

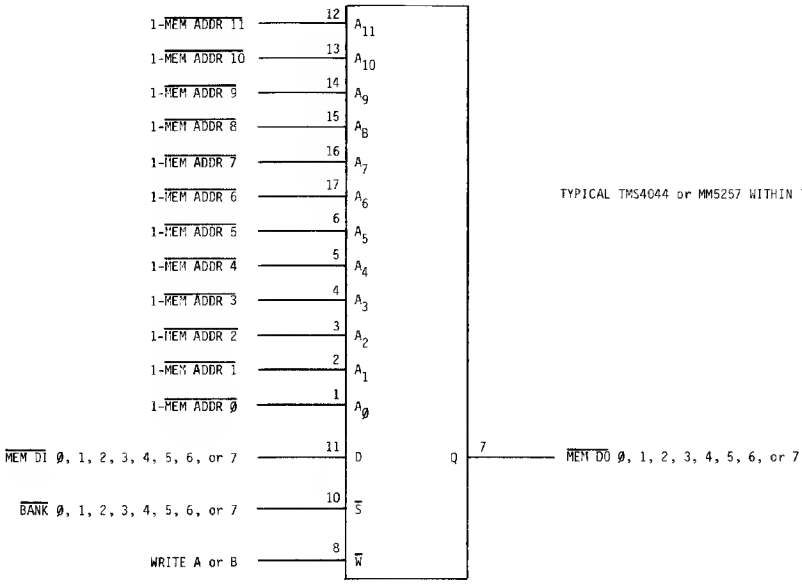


SUPERRAM 32K STATIC RAM PAGE 1 OF 2

BOARD SELECT LOGIC, ADDRESS AND DATA BUFFERS

	BIT 0	BIT 1	BIT 2	BIT 3		BIT 4	BIT 5	BIT 6	BIT 7	
BANK 0	1C	2C	3C	4C	BLOCK A	6C	7C	8C	9C	BLOCK A
BANK 1	1D	2D	3D	4D		6D	7D	8D	9D	
BANK 2	1E	2E	3E	4E		6E	7E	8E	9E	
BANK 3	1F	2F	3F	4F		6F	7F	8F	9F	
BANK 4	1H	2H	3H	4H	BLOCK B	6H	7H	8H	9H	BLOCK B
BANK 5	1J	2J	3J	4J		6J	7J	BJ	9J	
BANK 6	1K	2K	3K	4K		6K	7K	BK	9K	
BANK 7	1L	2L	3L	4L		6L	7L	BL	9L	

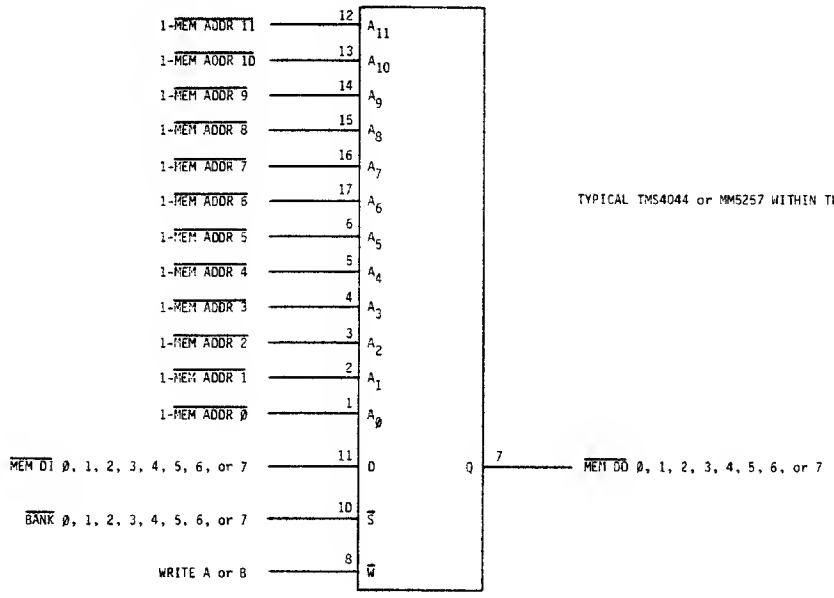
MEMORY ARRAY LAYOUT



TYPICAL TMS4044 or MM5257 WITHIN THE MEMORY ARRAY

	BIT 0	BIT 1	BIT 2	BIT 3		BIT 4	BIT 5	BIT 6	BIT 7	
BANK Ø	1C	2C	3C	4C	BLOCK A	6C	7C	8C	9C	BLOCK A
BANK 1	1D	2D	3D	4D		6D	7D	8D	9D	
BANK 2	1E	2E	3E	4E		6E	7E	8E	9E	
BANK 3	1F	2F	3F	4F		6F	7F	8F	9F	
BANK 4	1H	2H	3H	4H	BLOCK B	6H	7H	8H	9H	BLOCK B
BANK 5	1J	2J	3J	4J		6J	7J	8J	9J	
BANK 6	1K	2K	3K	4K		6K	7K	8K	9K	
BANK 7	1L	2L	3L	4L		6L	7L	8L	9L	

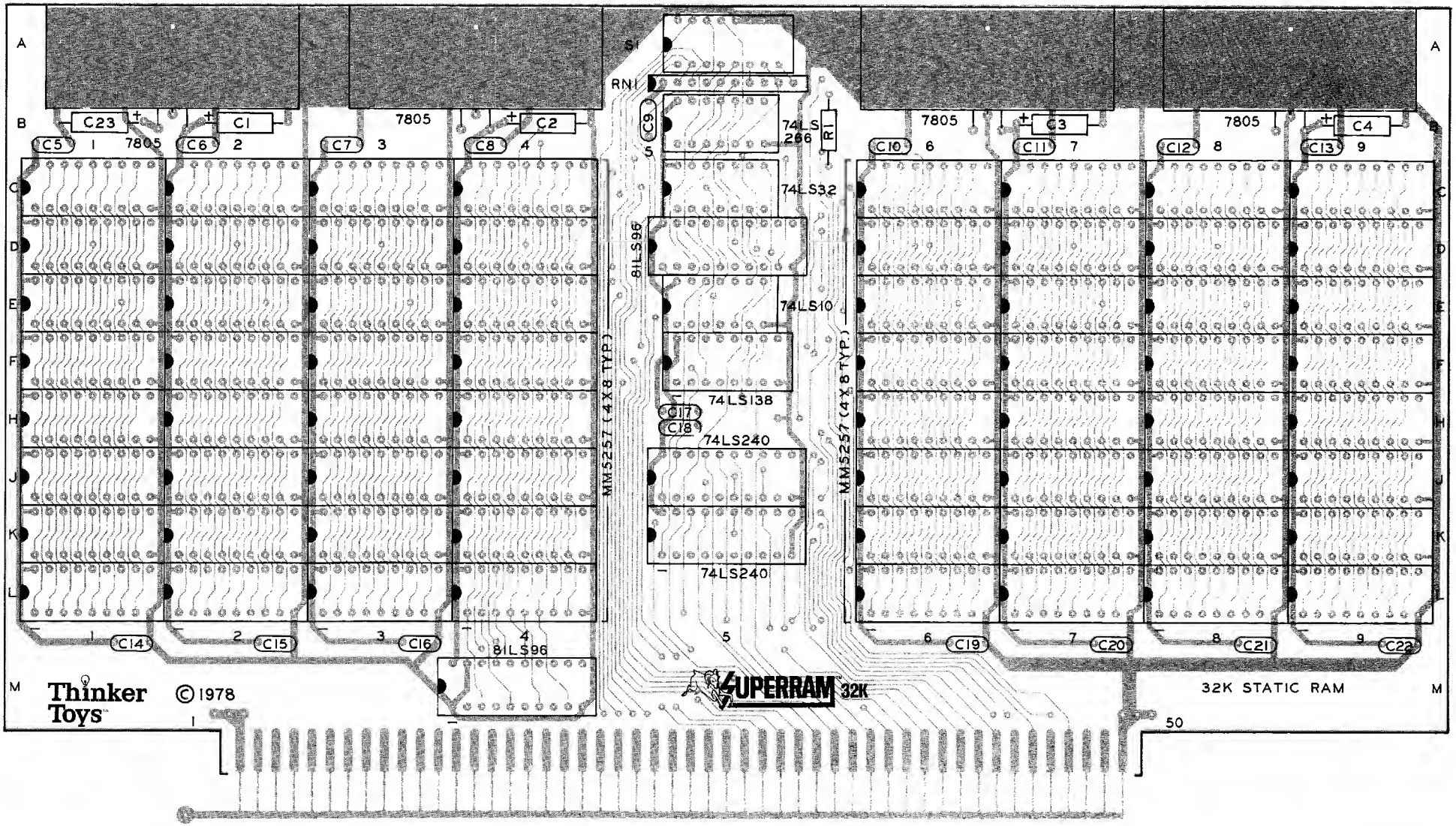
MEMORY ARRAY LAYOUT



TYPICAL TMS4044 or MM5257 WITHIN THE MEMORY ARRAY

SUPERRAM 32K STATIC RAM — PAGE 2 OF 2

MEMORY ARRAY LAYOUT AND MEMORY CHIP PINOUT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MM5257 (4X8 TYP.)
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